

November 20, 2002

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- Drafts
- Pending
- Active
 - L1: (1) ("5985126"). PN.
 - L2: (38349) noble
 - L3: (0) 11 and 12
 - L4: (91663) Platinum
 - L5: (1) 11 and 14
 - L6: (25948) noble adj (metal or metals)
 - L7: (0) 11 and 16
- Failed
- Saved
- Favorites
- Tagged (0)
- UDC
- Queue
- Trash

only maintained as contact point

Current: L1
DB: USPA
Default operator: GR

Print
History of item track

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U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	V	A	Item
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11/2002

201.09 Substitute Application

The use of the term "Substitute" to designate any application which is in essence the duplicate of an application by the same applicant abandoned before the filing of the later application, finds official recognition in the decision *Ex parte Komenak*, 1940 C.D. 1, 512 O.G. 739 (Comm'r Pat. 1940). Current practice does not require applicant to insert in the specification reference to the earlier application; however, attention should be called to the earlier application. The notation on the file wrapper (see MPEP § 202.02) that one application is a "Substitute" for another is printed in the heading of the patent copies. See MPEP § 202.02.

As is explained in MPEP § 201.11, a "Substitute" does not obtain the benefit of the filing date of the prior application.

Use form paragraph 2.07 to remind applicant of possible substitute status.

¶ 2.07 Definition of a Substitute

Applicant refers to this application as a "substitute" of Application No. [1], filed [2]. The use of the term "substitute" to designate an application which is in essence the duplicate of an application by the same applicant abandoned before the filing of the later case finds official recognition in the decision, *Ex parte Komenak*, 1940 C.D. 1, 512 O.G. 739 (Comm'r Pat. 1940). The notation on the file wrapper (See MPEP § 202.02) that one case is a "substitute" for another is printed in the heading of the patent copies. A "substitute" does not obtain the benefit of the filing date of the prior application.

201.10 Refile

No official definition has been given the term "Refile," though it is sometimes used as an alternative for the term "Substitute."

If the applicant designates his or her application as "Refile" and the examiner finds that the application is in fact a duplicate of a former application by the same party which was abandoned prior to the filing of the second application, the examiner should require the substitution of the word "substitute" for "refile", since the former term has official recognition.

Use form paragraph 2.08 to remind applicant of possible refile status.

¶ 2.08 Definition of a Refile

It is noted that applicant refers to this application as a "refile." No official definition has been given the term "refile," though it is sometimes used as an alternative for the term "substitute." Since this application appears to be in fact a duplicate of a former application which was abandoned prior to the filing of the second case, the substitution of the word "substitute" for "refile" is required since the term "substitute" has official recognition. Applicant is required to make appropriate corrections.

201.11 Continuity Between Applications: When Entitled to Filing Date

Under certain circumstances an application for patent is entitled to the benefit of the filing date of a prior nonprovisional application or provisional application which has at least one common inventor. The conditions are specified in 35 U.S.C. 120 and 35 U.S.C. 119(e).

35 U.S.C. 120. Benefit of earlier filing date in the United States.

An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States, or as provided by section 363 of this title, which is filed by an inventor or inventors named in the previously filed application shall have the same effect, as to such invention, as though filed on the date of the prior application, if filed before the patenting or abandonment of or termination of proceedings on the first application or on an application similarly entitled to the benefit of the filing date of the first application and if it contains or is amended to contain a specific reference to the earlier filed application. No

application shall be entitled to the benefit of an earlier filed application under this section unless an amendment containing the specific reference to the earlier filed application is submitted at such time during the pendency of the application as required by the Director. The Director may consider the failure to submit such an amendment within that time period as a waiver of any benefit under this section. The Director may establish procedures, including the payment of a surcharge, to accept an unintentionally delayed submission of an amendment under this section.

35 U.S.C. 119. Benefit of earlier filing date; right of priority.

(e)

(1) An application for patent filed under section 111(a) or section 363 of this title for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in a provisional application filed under section 111(b) of this title, by an inventor or inventors named in the provisional application, shall have the same effect, as to such invention, as though filed on the date of the provisional application filed under section 111(b) of this title, if the application for patent filed under section 111(a) or section 363 of this title is filed not later than 12 months after the date on which the provisional application was filed and if it contains or is amended to contain a specific reference to the provisional application. No application shall be entitled to the benefit of an earlier filed provisional application under this subsection unless an amendment containing the specific reference to the earlier filed provisional application is submitted at such time during the pendency of the application as required by the Director. The Director may consider the failure to submit such an amendment within that time period as a waiver of any benefit under this subsection. The Director may establish procedures, including the payment of a surcharge, to accept an unintentionally delayed submission of an amendment under this subsection during the pendency of the application

(2) A provisional application filed under section 111(b) of this title may not be relied upon in any proceeding in the Patent and Trademark Office unless the fee set forth in subparagraph (A) or (C) of section 41(a)(1) of this title has been paid.

(3) If the day that is 12 months after the filing date of a provisional application falls on a Saturday, Sunday, or Federal holiday within the District of Columbia, the period of pendency of the provisional application shall be extended to the next succeeding secular or business day.

There are six conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 or under 35 U.S.C. 119(e).

(A) The second application must be an application for a patent for an invention which is also disclosed in the first application (the parent or original nonprovisional application or provisional application); the disclosure of the invention in the first application and in the second application must be sufficient to comply with the requirements of the first paragraph of 35 U.S.C. 112. See *Transco Prods., Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994). Form paragraphs 2.09 and 2.10 should be used where the disclosure of the second application is not for an invention disclosed in the first application.

¶ 2.09 *Heading for Conditions for Domestic Priority Under 35 U.S.C. 119(e) or 120*

Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. [1] as follows:

Examiner Note

1.

In bracket 1, insert either or both --119(e)-- or --120--.

2.

One or more of the following form paragraphs 2.10 to 2.12 must follow depending upon the circumstances.

¶ 2.10 *Disclosure Must Be the Same*

The second application must be an application for a patent for an invention which is also disclosed in the first application (the parent or provisional application); the disclosure of the invention in the parent application and in the second application must be sufficient to

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	<u>1-43</u>	YES
	Claims	<u>NONE</u>	NO
Inventive Step (IS)	Claims	<u>5-7, 14, 38-42</u>	YES
	Claims	<u>1-4, 8-13, 15-37, 43</u>	NO
Industrial Applicability (IA)	Claims	<u>1-43</u>	YES
	Claims	<u>NONE</u>	NO

2. citations and explanations

Claims 1, 3, 35, 37 and 43 lack an inventive step under PCT Article 33(3) as being obvious over Zila et al (US 5,731,678 A) in view of Katou (US 5,344,491 A).

The Zila et al patent is directed to apparatus, shown in figure 2, for electroplating onto a semiconductor wafer. The apparatus is capable of electroplating material onto one surface of the wafer which is immersed in the electroplating solution while not exposing the opposite surface (column 1, lines 35-42). The apparatus includes a workpiece support with fingers 848 which provide electroplating power to the wafer at a plurality of discrete contact points about the periphery of the wafer as recited in instant claim 1. See figures 16-19, and column 15, line 30 to column 17, line 25. Seal 868 seals the electrode contact (column 19, lines 21-38).

The workpiece support is part of movable processing head 406 which spins about axis 410 (column 5, lines 50-57). The processing head includes an actuator which moves the head between a loading position, shown in figure 3, and a processing position, shown in figure 5, as recited in instant claim 3 (column 6, lines 3-46).

Applicant's claimed invention as recited in independent claims 1, 3 and 35 differs from the apparatus of Zila et al by reciting that the electroplating solution contains a noble metal and that an anode spaced from the workpiece support is provided. The Katou patent discloses a method and apparatus for electroplating a thin metal layer onto a semiconductor wafer 1 in which the wafer is positioned with the surface to be plated face down and exposed to the electroplating solution 4. Anode 7 is spaced from the workpiece within the electroplating solution (figure 2). One of the metals that may be plated is gold, a noble metal (column 5, line 10).

Applicant's claimed invention lacks an inventive step since it would have been obvious to have provided noble metal-containing electroplating solution in the apparatus of Zila et al because a noble metal such as gold is useful as a deposited layer on a semiconductor wafer as taught by Katou. It would additionally have been obvious to have provided an anode in the apparatus of Zila et al as shown by Katou to complete the circuit (Continued on Supplemental Sheet.)

Note newly cited references (page 12)

WRITTEN OPINION

Form PCT/IPEA/408 (Supplemental Box) (July 1998)
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International application No.

PCT/US00/29440

Supplemental Box

(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

Sheet 10

TIME LIMIT:

The time limit set for response to a Written Opinion may not be extended. 37 CFR 1.484(d). Any response received after the expiration of the time limit set in the Written Opinion will not be considered in preparing the International Preliminary Examination Report.

CLASSIFICATION:

The International Patent Classification (IPC) and/or the National classification are as listed below:
IPC(7): C25D 3/50, 5/02, 5/18, 7/12, 17/00, 21/06; H01L 21/288 and US Cl.: 204/199, 224R, 238; 205/123, 210, 264; 438/618

V. 2. REASONED STATEMENTS - CITATIONS AND EXPLANATIONS (Continued):

supplying electroplating power to the semiconductor wafer.

With respect to claim 37, figure 2 of Katou shows that the anode is in the form of a mesh through which the electroplating solution flows. The openings in the mesh serve as individual nozzles which provide fluid flow components to distribute the electroplating solution over the wafer as recited in instant claim 37. With respect to claim 43, there appears to be no separation of the electroplating solution of Katou as it flows toward the upper portion of the plating cup.

Claims 2, 4 and 36 lack an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Inoue et al (US 5,556,814 A).

Claims 2, 4 and 36 recite that the electroplating solution includes platinum for deposition on the workpiece. As noted above, Katou discloses that one of the metals that may be plated is gold. The Inoue et al patent is directed to the deposition of a metal layer on integrated circuits by electroplating. Inoue et al disclose that the electroplated metal may be copper, gold, platinum or palladium (column 6, lines 34-38). The claimed invention lacks an inventive step since it would have been obvious to have provided platinum in the electroplating solution of Zila et al because platinum is recognized as an equivalent to gold as shown by Inoue et al.

Claims 8 and 10-13 lack an inventive step under PCT Article 33(3) as being obvious over Zila et al (US 5,731,678 A) in view of Katou (US 5,344,491 A) as applied to claims 1, 3, 35, 37 and 43 above, and further in view of Tsuda et al (US 4,243,532 A) and Owczarz et al (US 5,232,328 A).

Zila et al and Katou are interpreted as above. Claim 8 additionally recites a chemical delivery system for supplying and recirculating electroplating solution and a multi-stage filtration system. Katou discloses a system for supplying electroplating solution to the plating chambers and recirculating the electroplating solution through filters 11. Katou does not specify multi-stage filtration. The Tsuda et al patent discloses apparatus in which a fluid is filtered. Tsuda et al teach that a plurality of filters having different pore sizes are placed within the flow path where the first filter has a large pore size to prevent large particles from flowing out and a successive filter has a smaller pore size to prevent finer powders from flowing out. By using this arrangement, clogging of the filter mesh becomes less frequent (column 5, line 57 to column 6, line 3). Choice of filter mesh sizes would have depended on size of particles determined to be detrimental to the process being carried out and the clogging frequency of the filters. This is illustrated by the Owczarz et al patent which is directed to apparatus for semiconductor processing. Owczarz et al suggest providing a first filter with an approximate pore size of 1 micron and a second filter with an approximate pore size of 0.1-0.2 microns to reduce introduction of contaminant particles into the processing chamber (column 18, lines 10-16). The claimed invention lacks an inventive step since it would have been obvious to have utilized multi-stage filtration in the apparatus of Owczarz et al as taught by Tsuda et al and Owczarz et al because clogging of the filter would have been less frequent and contamination of the process by fine particles would have been reduced.

Claim 9 lacks an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Inoue et al (US 5,556,814 A).

Inoue et al is interpreted as above. Claim 9 recites that the electroplating solution includes platinum for deposition on the workpiece. The claimed invention lacks an inventive step since it would have been obvious to have provided platinum in the electroplating solution of Zila et al because platinum is recognized as an equivalent to gold as shown by Inoue et al.

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Continuation of: Boxes I - VIII

Sheet 11

Claim 15 lacks an inventive step under PCT Article 33(3) as being obvious over Katou (US 5,344,491 A) in view of Dubin (US 5,972,192 A) and either of the Lowenheim text *Electroplating* or Goldberg (US 5,484,518 A).

As noted above, the Katou patent discloses a method for electroplating a thin metal layer onto a semiconductor wafer 1 in which the wafer is positioned with the surface to be plated face down and exposed to the electroplating solution 4. Anode 7 is spaced from the workpiece within the electroplating solution. Electroplating power is supplied between cathode 3, connected to wafer 1, and anode 7. See figure 2 and column 3, lines 15-27. One of the metals that may be plated is gold, a noble metal (column 5, line 10).

Applicant's claimed process differs from the method of Katou by reciting application of electroplating power using a low current density for a first period of time and the subsequent application of higher current for a second period of time. The Dubin patent is directed to a process for electroplating a layer of metal onto a semiconductor wafer. Dubin teaches that a thin seed layer is required on the surface of the wafer to carry current for electroplating (column 4, lines 19-21). The Lowenheim text discusses ~~for~~ electroplating workpieces on which a thin conductive layer has been deposited to carry electroplating current. Lowenheim teaches that the surface does not have the electrical conductivity of massive metals, so that electroplating must be started at low current densities until a fair thickness of electrodeposit is built up (page 418). The Goldberg patent is directed to a process of electroplating in which a thin conductive coating to carry electroplating current is first formed. Goldberg teaches that theoretically, a low initial current density should be preferred with current density increased as an initial deposit is formed, to prevent burn off of the thin coating (column 8, lines 15-19).

The prior art is indicative of the level of skill of one of ordinary skill in the art. The claimed invention lacks an inventive step since it would have been obvious to have performed the electroplating process of Katou by providing a seed layer as taught by Dubin because this layer would have provided electrical conductivity sufficient for electroplating to the surface of the workpiece, and to have used a low current density for a first period of time and then to have increased the current density as taught by Lowenheim and Goldberg because the low current density would have electrodeposited metal onto the surface slowly without burning the seed layer, and the subsequent current density would have allowed faster plating to reduce process time.

Claims 16-19 and 32-34 lack an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Young et al (US 4,705,606 A).

Claims 16-19 and 32-34 additionally differ by reciting pre-treatment before electroplating and spinning to remove electroplating solution. The Young et al patent is directed to electroplating electrical connections on integrated circuits. Young et al teach that the substrate should be prepared before electroplating (column 3, lines 25-45). Preparation may include rinsing in deionized water. Following treatment the wafer is spun dry. The substrate may also be treated in an acidic solution. The claimed invention lacks an inventive step since it would have been obvious to have pretreated the wafer in the electroplating process of Katou by rinsing in deionized water or an acidic solution and removing process liquids by spinning as taught by Young et al because contaminants on the wafer surface would have been removed and the wafer would have been dried.

Claim 20 lacks an inventive step under PCT Article 33(3) as being obvious over Katou (US 5,344,491 A) in view of Dubin (US 5,972,192 A) and either of the Lowenheim text *Electroplating* or Goldberg (US 5,484,518 A), as applied to claim 15 above, and further in view of Inoue et al (US 5,556,814 A).

Katou, Dubin, Lowenheim and Goldberg are interpreted as above. Claim 20 recites that the electroplating solution includes platinum for deposition on the workpiece. As noted above, Katou discloses that one of the metals that may be plated is gold, and the Inoue et al disclose that the electroplated metal may be copper, gold, platinum or palladium (column 6, lines 34-38). The claimed invention lacks an inventive step since it would have been obvious to have deposited platinum in the process of Katou because platinum is recognized as an equivalent to gold as shown by Inoue et al.

Claims 21-31 lack an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Abys (US 4,427,502 A). Claims 21-31 relate to process parameters used in the electrodeposition of platinum. The Abys patent is directed to a process for electroplating platinum and platinum alloys. The platinum concentration ranges from 0.005 molar to saturation (column 4, lines 40-41). This range includes the range recited in instant claim 21. The pH is preferably within the range of 10 to 12.5 (column 3, lines 53-57). This range includes the range of 11-12 recited in claim 24. Abys discloses that a preferred temperature range is 50° to 70° C. This range falls within the range of 40-80° C recited in claim 22 and includes 65°C as recited in claim 23. The Lowenheim text discloses a number of plating baths useful for platinum plating. In addition to alkaline bath U similar to that of Abys, Lowenheim discloses that acidic baths can be used. Bath T has a pH of 2 which falls within the range recited in instant claim 27. The amount of platinum in this bath is 5 g/l which falls within the range recited instant claim 28.

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Sheet 12

Abys discloses the use of a broad current density range including less than 50 ASF for low speed plating and 50-1000 ASF for high speed plating (column 4, lines 43-45). A current of 50 ASF approximately equals 50 mA/cm². Lowenheim discloses current densities ranging from 40-140 A/m² (4-14 mA/cm²). Neither Abys nor Lowenheim discloses the use of pulse current. Dubin et al disclose that pulse current as recited in instant claims 25 and 30 may advantageously be used for electroplating into the surface features of a semiconductor wafer. See the abstract. In the examples, Dubin et al use a plating current density in the range of 5-50 mA/cm². This range includes values similar to those disclosed by Abys and Lowenheim, and overlaps the ranges recited in instant claims 26 and 29. In example 1, a pulse frequency of about 1 to about 1000 Hz (1 to 1000 milliseconds) and a duty cycle of about 10% to about 90% was used. These ranges include the pulse parameters recited in instant claim 31.

Applicant's claimed invention lacks an inventive step since it would have been obvious at the time the invention was made to have utilized process parameters for the electrodeposition of platinum which are shown to be conventional by Abys, Lowenheim and Dubin because the semiconductor wafer would have been effectively plated.

Claims 5-7, 14 and 38-42 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest a contact member for conducting electroplating power to a microelectronic workpiece which includes a removable conductive surface material disposed about an exterior surface of a conductive member.

Claim 14 meets the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the apparatus as recited for plating a noble metal or alloy on a microelectronic workpiece, the apparatus including a disposable current thief which comprises conductive portions of a printed circuit board.

Claim 38-42 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the apparatus as recited in claim 37 which additionally includes the specific features of these dependent claims.

Claims 5-7, 14 and 38-42 meet the criteria set out in PCT Article 33(4), because the claimed subject matter has industrial applicability in the field of semiconductor processing.

----- NEW CITATIONS -----

- US 4,243,532 A (TSUDA et al) 06 January 1981, column 5, line 57-column 6, line 3.
- US 5,232,328 A (OWCZARA et al) 03 August 1993, column 18, lines 10-16.
- US 5,344,491 A (KATOU) 06 September 1994, figure 2.
- US 5,484,518 A (GOLDBERG) 16 January 1996, column 8, lines 13-29.
- US 5,731,678 A (ZILA et al) 24 March 1998, abstract.

2/2002 09/429,446

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- Pending
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 - L1: (477) ((205/123) or (205/157)). CCLs.
 - L2: (1724) damascene
 - L3: (30) 11 and 12
 - L4: (94076) gold
 - L5: (16) 13 and 14
- Failed
- Saved
- Favorites
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- UDC
- Queue
- Trash

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13 and 14

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U	I	Document ID	Issue Date	Pages	Title	Current OR	Current Ref	Retrieval C	Inventor	S	C	P	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	<input type="checkbox"/>	US 6319384 B1	20011120	12	Pulse reverse electrodeposition for	205/103	205/105;		Taylor, E. Jennings et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
2	<input type="checkbox"/>	US 6303014 B1	20011016		Electrodeposition of metals in small recesses using	205/103	205/105;		Taylor, E. Jennings et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
3	<input type="checkbox"/>	US 6297157 B1	20011002		Time ramped method for plating of high aspect ratio	438/687	205/102;		Lopatin, Sergey D. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
4	<input type="checkbox"/>	US 6270647 B1	20010807		Electroplating system having auxiliary electrode exterior	205/99	204/224R;		Graham, Lyndon W. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
5	<input type="checkbox"/>	US 6261433 B1	20010717		Electro-chemical deposition system and method of	205/96	204/230.2;		Bandau, Uziel	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
6	<input type="checkbox"/>	US 6235406 B1	20010522		Copper film including laminated impurities	428/620	205/157;		Uzoh, Cyprian E.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
7	<input type="checkbox"/>	US 6203684 B1	20010320		Pulse reverse electrodeposition for	205/103	205/105;		Taylor, E. Jennings et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
8	<input type="checkbox"/>	US 6143155 A	20001107		Method for simultaneous non-contact electrochemical	205/87	205/123;		Adams, John A. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
9	<input type="checkbox"/>	US 6132586 A	20001017		Method and apparatus for non-contact metal plating of	205/123	205/137;		Adams, John A. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
10	<input type="checkbox"/>	US 6126806 A	20001003		Enhancing copper electro-migration resistance	205/182	205/157;		Uzoh, Cyprian E.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
11	<input type="checkbox"/>	US 6107186 A	20000822		High planarity high-density in-field metallization	438/633	205/103;		Erb, Darrell M.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
12	<input type="checkbox"/>	US 6099712 A	20000808		Semiconductor plating bowl and method using anode	205/123	204/275.1;		Kitzdorf, Thomas L. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
13	<input type="checkbox"/>	US 6056864 A	20000502		Electropolishing copper film to enhance CMP throughput	205/222	205/157;		Cheung, Robin W.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
14	<input type="checkbox"/>	US 6004880 A	19991221		Method of single step damascene process for	438/692	205/93;		Lin, Yuan-Ching et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
15	<input type="checkbox"/>	US 6001234 A	19991214		Methods for plating semiconductor workpieces	205/123	205/133;		Batz, Jr., Robert W. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
16	<input type="checkbox"/>	US 5965126 A	19991116		Semiconductor plating system workpiece support having	205/123	204/224R;		Bleck, Martin C. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

metal deposited in the trenches

DEPR: FIG. 4A illustrates schematically a cross-section of a semiconductor wafer that has been cut from a single crystal of a semiconductor, e.g., silicon. Such wafers are typically round and very thin. In order to metallize the surface of the wafer, a barrier layer (not shown) and a very thin conducting layer (not shown) are deposited, e.g., by CVD, as for the case of the ~~semiconductor~~ ^{semiconductor} prepared surface discussed above.

DEPA: FIG. 4B shows an enlarged cross section of the edge of the water 400 as indicated by the circle 4B in FIG. 4A. A metal layer 406 is shown schematically and with exaggerated thickness as deposited on the surface 402 of the water 300 near its edge 404 after the first, relatively short, cathodic current pulse. As discussed above for the $\text{Fe}(\text{NH}_4)_2(\text{SO}_4)_2$ -prepared surface, because the cathodic pulse is of finite duration, there may be some non-uniformity in the deposition of the metal layer, as shown by the excess metal 408 deposited at the edge 404 of the water 400.

DEPR: The method of the invention may be used with any metal that can be deposited by electroplating techniques. Thus copper, silver, gold, zinc, chromium, nickel, and alloys thereof such as bronzes, brass, and the like, may be applied to microcircuit surfaces by the process of the invention. The invention is particularly useful in filling trenches and vias in semiconductor "prepared surfaces" in the manufacture of VLSI semiconductor devices and the like and in preparing plane layers of metal on large-diameter semiconductor wafers.

The electroplating bath used in the process of the invention can be any conventional electroplating bath appropriate for the metal being plated. For electroplating copper onto a semiconductor surface, particularly when preplating macroscopic conductors by the laminate process, it is preferred to avoid conventional additives such as leveling agents and the like to the extent possible, in order to avoid the difficulties of using such additives such as possible inclusion in the plated conductors. A preferred bath for electroplating copper onto a macrorough surface is an aqueous acidic copper sulfate bath incorporating about 40 to about 80 g/L of copper sulfate, a molar ratio of sulfuric acid to copper sulfate of about 5:1 to about 8:1, about 58 or polyethylene glycol and about 30 ppm to about 60 ppm of chloride ion. A pulse train frequency of about 1000 Hz with a cathodic duty cycle of about 20%, an anodic duty cycle of about 75% and a cathodic/anodic charge transfer ratio of 5 or less appeared to give superior results.

CLER: 45. The method of claim 1 wherein said metal is selected from the group consisting of copper, silver, gold, zinc, chromium, nickel, bronze, brass, and alloys thereof.

Ad 4/5-4 has black 1-2 mm transverse

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(45) Date of Patent: Mar. 20, 2001

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Primary Examiner—Kathryn DeGros
Assistant Examiner—Wesley A. Nichols

(14) *Anwar, Agni, or Elm—Vet's, Suez, Sejmour, etc.*
Peace LLP

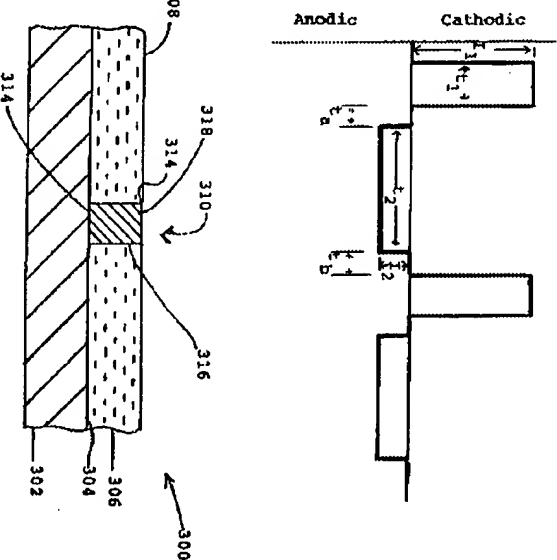
A smooth layer of a metal is electrodeposited onto a microrough electrically conducting substrate by immersing the substrate

to be electroplated and passing a modulated reversing electro current between the electrodes. The current contained

pulses that are anodic with respect to solid substrate. These cathodic pulses have a duty cycle less than about 50% and said anodic pulses have a duty cycle greater than about 50%.

pulses is greater than one, and the frequency of said pulses ranges from about 10 Hertz to about 5000 Hertz.

21 Claims, 4 Drawing Sheets



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DOCUMENT IDENTIFIER: US 6107186 A
TITLE: High planarity high-density in-laid metallization patterns by damascene - CMP processing

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ABSTRACT:
Erosion of high density metallization areas associated with conventional damascene - CMP processing is avoided and greater planarity achieved by selectively increasing the metal overburden layer thickness at high density metallization regions. Embodiments include initially filling recesses formed in the substrate surface with a metal forming a blanket or overburden layer of the metal thereon. Regions of the blanket or overburden layer overlying regions of high density metallization are selectively electroplated to a greater thickness. The surface is then planarized by CMP, with the selectively increased thickness areas of the overburden layer compensating for greater erosion rates thereof during CMP, thereby resulting in greater planarity of the polished surface.

BACKGROUND:
This invention relates to a method for forming metal films as part of high-density metallization processing of particular utility in integrated circuit semiconductor device and circuit board manufacture, which process employs "damascene" (or "in-laid") technology.

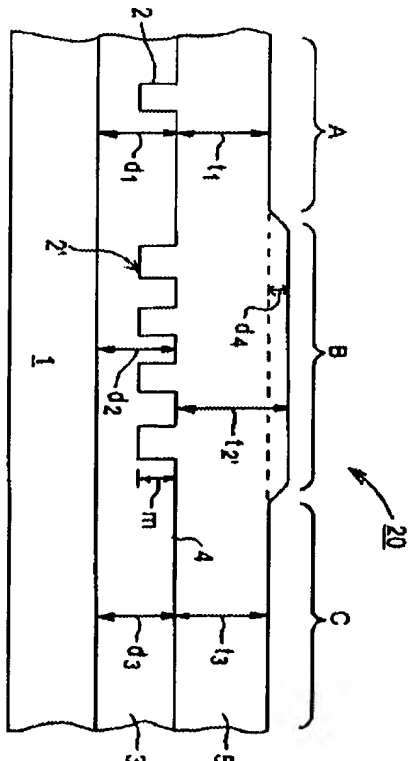
BRIEF DESCRIPTION OF THE DRAWINGS:
Metal films of the type contemplated herein are used, e.g., in "back-end" semiconductor manufacturing technology, to form electrically conductive contacts to active as well as passive device regions or components formed in or on a semiconductor substrate, as well as for filling via holes, interlevel metallization, and interconnection routing patterns for wiring together the components and/or regions. Metals employed for such purposes include, inter alia, titanium, tantalum, tungsten, aluminum, chromium, nickel, cobalt, silver, gold, copper, and their alloys. Of these, copper and copper-based alloys are particularly attractive for use in large-scale integration (LSI), very large-scale integration (VLSI), and ultra large-scale integration (ULSI) semiconductor devices requiring multilevel metallization systems for "back-end" processing of the semiconductor wafers on which the devices are based. Copper and copper-based metallization systems have very low resistivities, i.e., lower than those of previously preferred systems utilizing aluminum and its alloys, as well as significantly higher resistance to electromigration. Moreover, copper and its alloys enjoy a considerable cost advantage over a number of the above-mentioned metals, notably silver and gold. Also, in contrast to aluminum and the refractory-type metals included in the above listing, copper and its alloys can be readily deposited in good quality, bright layer form by well-known electroplating techniques, at deposition rates fully compatible with the requirements of device manufacturing throughput.

BRIEF DESCRIPTION OF THE DRAWINGS:
Referring now to FIG. 1, schematically shown therein in cross-sectional view is a conventional damascene processing sequence for forming recessed (i.e.,

United States Patent [19]
Erb [11] Patent Number: 6,107,186
[45] Date of Patent: Aug. 22, 2000

[54] HIGH PLANARITY HIGH-DENSITY IN-LAID METALLIZATION PATTERNS BY DAMASCENE-CMP PROCESSING
[73] Inventor: Darrell M. Erb, Los Altos, Calif.
Assignee: Advanced Micro Devices, Inc., Sunnyvale, Calif.
[21] Appl. No.: 09/238,051
[22] Filed: Jan. 27, 1999
[31] Int. Cl.⁷: H01L 21/673
[32] U.S. Cl.: 438/633; 438/687; 438/692; 438/694; 438/695; 438/696; 438/697; 438/698; 438/699; 438/700; 438/701; 438/702; 438/703; 438/704; 438/705; 438/706; 438/707; 438/708; 438/709; 438/710; 438/711; 438/712; 438/713; 438/714; 438/715; 438/716; 438/717; 438/718; 438/719; 438/720; 438/721; 438/722; 438/723; 438/724; 438/725; 438/726; 438/727; 438/728; 438/729; 438/730; 438/731; 438/732; 438/733; 438/734; 438/735; 438/736; 438/737; 438/738; 438/739; 438/740; 438/741; 438/742; 438/743; 438/744; 438/745; 438/746; 438/747; 438/748; 438/749; 438/750; 438/751; 438/752; 438/753; 438/754; 438/755; 438/756; 438/757; 438/758; 438/759; 438/760; 438/761; 438/762; 438/763; 438/764; 438/765; 438/766; 438/767; 438/768; 438/769; 438/770; 438/771; 438/772; 438/773; 438/774; 438/775; 438/776; 438/777; 438/778; 438/779; 438/780; 438/781; 438/782; 438/783; 438/784; 438/785; 438/786; 438/787; 438/788; 438/789; 438/790; 438/791; 438/792; 438/793; 438/794; 438/795; 438/796; 438/797; 438/798; 438/799; 438/800; 438/801; 438/802; 438/803; 438/804; 438/805; 438/806; 438/807; 438/808; 438/809; 438/810; 438/811; 438/812; 438/813; 438/814; 438/815; 438/816; 438/817; 438/818; 438/819; 438/820; 438/821; 438/822; 438/823; 438/824; 438/825; 438/826; 438/827; 438/828; 438/829; 438/830; 438/831; 438/832; 438/833; 438/834; 438/835; 438/836; 438/837; 438/838; 438/839; 438/840; 438/841; 438/842; 438/843; 438/844; 438/845; 438/846; 438/847; 438/848; 438/849; 438/850; 438/851; 438/852; 438/853; 438/854; 438/855; 438/856; 438/857; 438/858; 438/859; 438/860; 438/861; 438/862; 438/863; 438/864; 438/865; 438/866; 438/867; 438/868; 438/869; 438/870; 438/871; 438/872; 438/873; 438/874; 438/875; 438/876; 438/877; 438/878; 438/879; 438/880; 438/881; 438/882; 438/883; 438/884; 438/885; 438/886; 438/887; 438/888; 438/889; 438/890; 438/891; 438/892; 438/893; 438/894; 438/895; 438/896; 438/897; 438/898; 438/899; 438/900; 438/901; 438/902; 438/903; 438/904; 438/905; 438/906; 438/907; 438/908; 438/909; 438/910; 438/911; 438/912; 438/913; 438/914; 438/915; 438/916; 438/917; 438/918; 438/919; 438/920; 438/921; 438/922; 438/923; 438/924; 438/925; 438/926; 438/927; 438/928; 438/929; 438/930; 438/931; 438/932; 438/933; 438/934; 438/935; 438/936; 438/937; 438/938; 438/939; 438/940; 438/941; 438/942; 438/943; 438/944; 438/945; 438/946; 438/947; 438/948; 438/949; 438/950; 438/951; 438/952; 438/953; 438/954; 438/955; 438/956; 438/957; 438/958; 438/959; 438/960; 438/961; 438/962; 438/963; 438/964; 438/965; 438/966; 438/967; 438/968; 438/969; 438/970; 438/971; 438/972; 438/973; 438/974; 438/975; 438/976; 438/977; 438/978; 438/979; 438/980; 438/981; 438/982; 438/983; 438/984; 438/985; 438/986; 438/987; 438/988; 438/989; 438/990; 438/991; 438/992; 438/993; 438/994; 438/995; 438/996; 438/997; 438/998; 438/999; 439/000

[36] Field of Search: 205/35, 123, 103, 205/104, 116, 125, 438/692, 633, 687, 216/88, 527/98, 59, 250, 430.1, 443.1
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- ☐ Drafts
- ☒ Pending
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- ☒ L1: (253) ("205/123").CCLS.
- ☒ L3: (119) ("205/124").CCLS.
- ☒ L5: (364) 11 or 13
- ☒ L7: (105621) platinum or Pt
- ☒ L9: (107) 15 and 17
- ☒ L11: (67) 11 and 17
- ☒ L13: (515947) raise or raises or raised or rising
- ☒ L15: (1560562) increase or increases or increased or incr
- ☒ L17: (8988) 113 near1 (voltage or current)
- ☒ L19: (65271) 115 near1 (voltage or current)
- ☒ L21: (1397) seed adj layer
- ☒ L23: (4) 117 and 121
- ☒ L25: (71) 119 and 121

- ☒ Failed
- ☒ saved
- ☒ Favorites
- ☒ Tagged
- ☒ UDC
- ☒ Queue
- ☒ Trash

DB: ASPAT
Detail: ASPAT OR
119 and 121
[Details] [Close] [Queue] [Clear]
[Print] [Synonyms]
[Highlight all items]

U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XREF	Retrieval C	Inventor	S	C	P	A	J	S

#8 6,162,344 12/2000 [9/1998] DIV 6,070,544 Able to allow current resistive drop, negligible, the increase current
cd 1130 seed layer cd 1225+, 146 cd 601 cd 120 5.25mBlower - 475mBlower cd 15447 cd 3
#14 6,110,346 6/1999 [7/1998] Similar to #8
#19 6,070,544 6/1999 [7/1998] Same as #8
#15 6,101,602 6/1999 [7/1998] TSM chip upper defect cd 1136 avoid unbleeding - suspended with layer comp cd 8,134 interest current
#12 5,605,615 6/1999 M-faults Able plotting power supply circuitry - allows voltage to be revised cd 10442

- ☒ Drafts
- ☐ Pending
- ☐ Active

- BR1: 1
- L1: (253) ("205/123").CCLS.
- L3: (119) ("205/124").CCLS.
- L5: (364) 11 or 13
- L7: (105621) platinum or Pt
- L9: (107) 15 and 17
- L11: (67) 11 and 17
- L13: (516947) raise or raises or raised or rising
- L15: (1560562) increase or increases or increased or incr
- L17: (8988) 113 near1 (voltage or current)
- L19: (65271) 115 near1 (voltage or current)
- L21: (1397) seed adj layer
- L25: (71) 119 and 121
- L23: (4) 117 and 121
- L27: (1) 117 and 15
- L29: (30) 119 and 15
- L31: (31) 127 of 129

- ☐ Saved
- ☐ Favorites
- ☐ Tagged
- ☐ UDC
- ☐ Queue
- ☐ Trash

127 of 129

127 of 129

127 of 129

U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XREF	Retrieval C	Inventor	S	C	P	3	3	3	3	3	3	3
1	<input checked="" type="checkbox"/>	US 6171467 B1	20010109	9	Electrochemical-control of abrasive polishing and	205/93	156/345	204/224M	Weins, Timothy P. et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
2	<input checked="" type="checkbox"/>	US 6132585 A	20001017		Semiconductor element and method and apparatus for	205/123	136/258	136/290	Nicotikawa, Takafumi et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
3	<input checked="" type="checkbox"/>	US 6123824 A	20000926		Process for producing photo-electricity generating	205/124	205/333		Sano, Masafumi et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
4	<input checked="" type="checkbox"/>	US 6113771 A	20000905		Electro deposition chemistry	205/123	106/1.22	106/1.25	Landau, Uziel et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
5	<input checked="" type="checkbox"/>	US 6066246 A	20000523		Cylindrical edged microstrip transmission line and method	205/123			Richards, Randy J. et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
6	<input checked="" type="checkbox"/>	US 5980720 A	19991109		Method of treating crystal-grown wafers for	205/118	205/120	205/123	Park, Jung-min et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
7	<input checked="" type="checkbox"/>	US 5834995 A	19981110		Cylindrical edge microstrip transmission line	333/238	205/123		Richards, Randy J. et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
8	<input checked="" type="checkbox"/>	US 5747355 A	19980505		Method for producing a transistor using anodic	438/163	205/124	438/303	Konuma, Toshimitsu et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
9	<input checked="" type="checkbox"/>	US 5747180 A	19980505		Electrochemical synthesis of quasi-periodic quantum dot	428/601	205/124	205/173	Miller, Albert E. et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
10	<input checked="" type="checkbox"/>	US 5731216 A	19980324		Method of making an active matrix display incorporating	438/30	205/123	257/59	Holmberg, Scott H. et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
11	<input checked="" type="checkbox"/>	US 5728592 A	19980317		Method for fabricating a thin film transistor matrix	438/161	205/123	257/59	Oki, Ken-ichi et al.	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
12	<input checked="" type="checkbox"/>	US 5679234 A	19971021		Process of forming miniature	205/123	204/192.34		Imamura, Takafumi	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Drafts

BRS: 1

Active

- L1: (253) ("205/123").CCLS.
- L3: (119) ("205/124").CCLS.
- L5: (364) 11 or 13
- L7: (105621) platinum or Pt
- L9: (107) 15 and 17
- L11: (67) 11 and 17
- L13: (516947) raise or raises or raised or rising
- L15: (1560562) increase or increases or increased or inc
- L17: (8988) 113 near1 (voltage or current)
- L19: (65271) 115 near1 (voltage or current)
- L21: (1397) seed adj Layer
- L25: (71) 119 and 121
- L23: (4) 117 and 121
- L27: (1) 117 and 15
- L29: (30) 119 and 15
- L31: (31) 127 or 129
- L33: (38593) 438/5.ccls.
- L35: (19150) electroplats.
- L37: (10983) electrodeposits
- L39: (73992) electrolyts
- L41: (91195) 135 or 137 or 139
- L43: (168) 141 same 117
- L45: (1876) 141 same 119
- L47: (2006) 143 or 145
- L49: (35) 147 and 133

checked all 35

pdfs: 100% 100% 100% 100%

Detail: 100% 100%

L47 and 133

100% 100% 100% 100%

U	1	Document ID	Issue Date	Pages	Title	Current OR	Current KRIF	Retrieval C	Inventor	S	C	P	3	5
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Details

Head

NUM

- ☐ Dratris
- ☐ Pending
- ☒ Active
 - L1: (77647) wafer or wafers
 - L2: (83347) spin or spun
 - L3: (1735) 12 near2 dry
 - L4: (427) 11 and 13
 - L5: (281) 11 same 13
 - L6: (86905) rinse or rinses or rinsed or rinsing
 - L7: (213) 16 same 15
 - L8: (13209) 205/50-333.ccls.
 - L9: (6) 17 and 19
- ☐ Failed
- ☐ Saved
- ☐ Favorites
- ☐ Tagged
- ☐ UDC
- ☐ Queue
- ☐ Trash

DB: 35PAT
 Detail operator: OR
 17:and=18
 Bowed Queue Date

☐ Date
☐ Highlight all items fully

U	Document ID	Issue Date	Pages	Title	Current OR	Current XREF	Retrieval C	Inventor	S	C	P	3	3
<input type="checkbox"/>	US 6179982 B1	20010130	29	Introducing and reclaiming liquid in a wafer processing	205/80	204/224M		Ting, Chiu H.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	US 6077412 A	20000620		Rotating anode for a wafer processing chamber	205/143	204/212		Ting, Chiu H.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	US 5755944 A	19980526		Formation of layer having openings produced by process for patterned electroplating	204/486	204/490		Haven, Duane A.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	US 5545307 A	19960813		Patterned electroplating	205/122	430/320		Doss, Saad K.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	US 5516418 A	19960514		Groundplane post-etch andolization	205/119	205/122		Doss, Saad K.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	US 4514254 A	19850430			205/125	205/109		Klepner, Stephen P.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

US 6179982 B1 20010130 29 pages
 US 6077412 A 20000620
 US 5755944 A 19980526
 US 5545307 A 19960813
 US 5516418 A 19960514
 US 4514254 A 19850430
 US 6179982 B1 20010130 29 pages

- 11: (77647) wafer or wafers
- 12: (83347) spun or spun
- 13: (1735) 12 near2 dry
- 14: (427) 11 and 13
- 15: (201) 11 same 13
- 16: (86905) rinse or rinses or rinsed or rinsing
- 17: (213) 16 same 15
- 18: (13209) 205/50-333.ccls.
- 19: (6) 17 and 18
- 110: (5) ("4285784") or ("4427502") or ("5320978") or ("
- 111: (255) ("205/123").ccls.
- 112: (79446) (low or lower) near1 voltage
- 113: (27966) (low or lower) near1 current
- 114: (113480) (high or higher) near1 voltage
- 115: (44757) (high or higher) near1 current
- 116: (181732) 112 or 113 or 114 or 15
- 117: (34) 111 and 116 (bale1 v) 34
- 118: failed
- 119: saved
- 120: favorites
- 121: tagged
- 122: udc
- 123: queue
- 124: trash

This image shows a blank sheet of lined paper, likely a template for a student exercise or report. On the left side, there is a vertical margin containing four rectangular boxes stacked vertically. Each box has a label in German: "Ab OEG Name", "Ab ISAR from", "Zeichnung", and "Ein Text". The rest of the page is filled with horizontal ruling lines. At the bottom right corner, there is a small square box containing the number "1".

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current Knef	Retrieval C	Inventor	S	C	P	3	5
1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6197181 B1	20010306	18	Apparatus and method for electrolytically depositing	205/123	204/198 ; 205/183		Chen, Linlin	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6193870 B1	20010227		Use of a hard mask for formation of gate and	205/123	205/664 ; 445/50		Morse, Jeffrey D. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6174425 B1	20010116		Process for depositing a layer of material over a	205/96	204/297.01 ; 204/DIG.7		Simpson, Cindy Reidsma	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6171052 B1	20010109		Methods of forming metallization layers and	438/641	205/123 ; 205/125		sandhu, Gurej sandhu et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6066246 A	20000523		Cylindrical edged microstrip transmission line and method	205/123			Richards, Randy J. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
6	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6045678 A	20000404		Formation of nanofilament field emission devices	205/123	445/50		Morse, Jeffrey D. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5972192 A	19991026		Pulse electroplating copper or copper alloys	205/101	205/103 ; 205/104		Dubin, Valery et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
8	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5968333 A	19991019		Method of electroplating a copper or copper alloy	205/184	205/123 ; 205/164		Nogami, Takeshi et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
9	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5882498 A	19990316		Method for reducing oxidation of electroplating	205/261	205/123 ; 205/157		Dubin, Valery et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
10	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5834995 A	19981110		Cylindrical edge microstrip transmission line	333/238	205/123		Richards, Randy J. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
11	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5662788 A	19970902		Method for forming a metallization layer	205/87	205/103 ; 205/118		sandhu, Gurej sandhu et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
12	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5595637 A	19970121		Photoelectrochemical	205/91	205/123		Trench, D. Morgan	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

	σ_{eff}
# 23	5.2 uL, 56.9 g/mL contact cell, cu8d/v2, 1st g/L eqv. c' v.0.1 m/m water per mol g/l ⁻¹ , 1st c' 0.03-0.05 M/m ²

☐ Drafts
☐ Pending
☒ Active

- U1: (10000) water or water's
L3: (1735) 12 near2 dry
L4: (427) 11 and 13
L5: (281) 11 same 13
L6: (86905) rinse or rinses or rinsed or rinsing
L7: (213) 16 same 15
L8: (13209) 205/50-333.ccls.
L9: (6) 17 and 18
L10: (5) ("4285784" or ("4427502") or ("5320978") or ("205/123").CCLs.
L11: (255) ("205/123").CCLs.
L12: (79446) (low or lower) nearl voltage
L13: (27966) (low or lower) nearl current
L14: (113480) (high or higher) nearl voltage
L15: (44757) (high or higher) nearl current
L16: (181732) 112 or 113 or 114 or 15
L17: (34) 111 and 116
L18: (13209) 205/50-333.ccls.
L19: (15996) 116 same (semiconductor or semiconductors
L20: (70) 118 and 119
L21: (61) 120 not 117
- ☐ Failed
☐ Saved
☐ Favorites
☐ Tagged
☐ UDC

120 not 117

Area for document content or image.

U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	3	7
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..#4 6,144,724 | Als. dep. in 21494 low current; then high current 415/1m4

☐ Drafts ☐ Pending ☒ Active

☐ L1: (77647) water or wafers
☐ L2: (83347) spin or spun
☐ L3: (1735) 12 near2 dry
☐ L4: (427) 11 and 13
☐ L5: (281) 11 same 13
☐ L6: (86905) rinse or rinses or rinsed or rinsing
☐ L7: (213) 16 same 15
☐ L8: (13209) 205/50-333.ccls.
☐ L9: (6) 17 and 18
☐ L10: (5) ("4285784") or ("427502") or ("5320978") or
☐ L11: (255) ("205/123").CCLS.
☐ L12: (79446) (low or lower) near1 voltage
☐ L13: (27966) (low or lower) near1 current
☐ L14: (113480) (high or higher) near1 voltage
☐ L15: (44757) (high or higher) near1 current
☐ L16: (181732) 112 or 113 or 114 or 15
☐ L17: (34) 111 and 116
☐ L18: (13209) 205/50-333.ccls.
☐ L19: (15996) 116 same (semiconductor or semiconductors
☐ L20: (70) 118 and 119
☐ L21: (61) 120 not 117
☐ L22: (5672) 11 same 12
☐ L23: (9) 122 and 111

Default operator: OR

DB: USPAT

Booze Queue Date

☐ Photo ☐ Screen

Document ID	Issue Date	Pages	Title	Current OR	Current XREF	Retrieval C	Inventor	S	C	P	3	3	3
US 6187164 B1	20010213	12	Method for creating and testing a combinatorial semiconductor plating bowl and method using anode	205/81	205/118 ; 205/122		Warren, Christopher J. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
US 6099712 A	20000808		Semiconductor plating bowl and method using anode	205/123	204/275.1 ; 204/286.1		Ritzdorf, Thomas L. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
US 6001234 A	19991214		Methods for plating semiconductor workpieces	205/123	205/143 ; 205/291		Batz, Jr., Robert W. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
US 5385126 A	19991116		Semiconductor plating system	205/123	204/224R ; 204/288.1		Bleck, Martin G. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
US 5980706 A	19991109		Workpiece support having electrode semiconductor workpiece holder	204/297.14	118/729 ; 118/730		Bleck, Martin et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
US 5746903 A	19980505		Wet chemical processing techniques for plating high pseudo-electroless, followed by electroless, thin-film electrical connections for integrated	205/118	205/123 ; 205/125 ; 205/123		Beilin, Solomon I. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
US 5284107 A	19931123			205/86	205/118 ; 205/123		Bentson, Richard S. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
US 4705606 A	19871110			205/123	257/698 ; 257/706		Young, Peter L. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

CA 3,335 surface prep then wash with spin dry